

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S3	27537	memory same attribut\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 17:49
S4	25686	(FPGA programmable adj logic )same implement\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 17:50
S5	833	S3 and S4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 17:51
S7	51	S5 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 17:52
S6	1776	specification same logical same description	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 17:52
S8	4	S5 and S6 and physical and interconnect\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:05
S9	109	programmable adj architecture same implement\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:06
S10	0	programmable adj architecture same implement\$5 and logical with description	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:07

## EAST Search History

S11	31	programmable adj architecture same implement\$5 and logical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:09
S12	0	programmable adj architecture same implement\$5 and logical and attribute with memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:10
S14	61990	(FPGA programmable adj logic)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:11
S13	55154	memory adj system	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:11
S15	243	attribut\$3 same logical adj (description data information)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:13
S16	0	S13 and S14 and S15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:14
S17	8262	memory adj system same implement\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:15
S18	788	specification same attribute same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:16

## EAST Search History

S19	16	S17 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:17
S20	12	S17 and S18 and logical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:19
S21	12	S17 and S18 and logical and physical	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:20
S30	71	memory same specification same attribute and implement\$5 and logic\$2 same (data description information \$HDL verilog hardware adj description adj language) and (receiv\$3 obtain\$3 input\$4 determin\$3) and interconnect\$3 and (FPGA programmable PLD) and generat\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:29
S31	59	memory same specification same attribute and implement\$5 and logic\$2 same (data description information \$HDL verilog hardware adj description adj language) and (receiv\$3 obtain\$3 input\$4 determin\$3) and interconnect\$3 and (FPGA programmable PLD) and generat\$3 and @ad<"20040101"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:32
S32	190	specification same attribute same memory with (circuit system)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:34
S33	1315	generat\$5 same logical same description same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:35

## EAST Search History

S35	55154	memory adj system	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:36
S34	2	S32 and S33	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:36
S38	2	(FPGA CLB PLD programmable adj logic adj device) and interconnect adj structure and memory and message adj processing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:44
S39	49	(FPGA CLB PLD programmable adj logic adj device) and interconnect adj structure and memory and receiv\$3 same specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:45
S37	1061	(FPGA CLB PLD programmable adj logic adj device) and interconnect adj structure and memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:45
S42	6	(FPGA CLB PLD programmable adj logic adj device) and interconnect same structure and memory and receiv\$3 same specification same attribute and implement\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:49
S43	5	(FPGA CLB PLD programmable adj logic adj device) and interconnect same structure and memory and receiv\$3 same specification same attribute and implement\$5 and generat\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:51
S46	2	(FPGA CLB PLD programmable adj logic adj device) and interconnect same structure and memory and receiv\$3 same specification same attribute and implement\$5 and generat\$3 same ( layout physical)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/11 18:52

## EAST Search History

S54	5997	memory near3 attribute	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 13:14
S56	259	S54 and S55	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 13:15
S57	26203	memory same interconnect\$3 same component	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 13:16
S73	62	memory adj system and specification and attribute and logical and (layout physical) and interconnect\$3 with topology and @ad<"20040101"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 13:33
S75	6	memory adj system and specification and attribute and logical and (layout physical) and interconnect\$3 with topology and @ad<"20040101" and "716"/\$.ccls. and memory with ( design\$3 architecture interconnection network)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 13:35
S74	6	memory adj system and specification and attribute and logical and (layout physical) and interconnect\$3 with topology and @ad<"20040101" and "716"/\$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 13:35
S61	28	S56 and S57 and (layout physical) and topology	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 13:44
S58	57	S56 and S57	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 13:44

## EAST Search History

S78	482225	memory with system	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 15:49
S80	16298	S78 and S79	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 15:51
S79	102118	(receiv\$3 input\$4 obtain\$3 provid\$3) with specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 15:51
S82	622	S80 and S81	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 15:52
S81	14804	memory with attribute	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 15:52
S84	579	S82 and S83	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 16:00
S83	5042196	generat\$3 logical adj description same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 16:00
S85	233	generat\$3 same (physical layout) adj description	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 16:01

## EAST Search History

S86	3	S84 and S85	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/18 16:04
S90	718	(generat\$3 provid\$3 output\$4 ) with ( logical description representation netlist HDL behavioral) same memory near\$4 (component interconnect\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 17:30
S91	257517	(physical layout) with (representation description data information output input)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 17:32
S10 4	0	S89 and S90 and S91 and S102	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 17:46
S10 3	1	S89 and S90 and S91	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 17:46
S89	791	specification same attribute same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 18:08
S10 9	38	specification same attribute and memory and (message adj processing network) and (logical adj (description representation data)) same generat\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 18:11
S10 7	6	specification same attribute same memory and (message adj processing network) and (logical adj (description representation data)) and generat\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 18:11

## EAST Search History

S10 2	89	interconnect\$5 with topology same component same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 18:16
S11 5	205	memory same component same attribute and interconnect\$3 and (description representation netlist HDL verilog hardware adj description data information output) same ( logical physical layout ) same( configuration topology)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 18:21
S11 2	174	memory same component same attribute and interconnect\$3 and (description representation netlist HDL verilog hardware adj description data information output) same ( logical physical layout ) and topology	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 18:25
S11 8	40	generat\$3 with logical adj2 (representation description information data) and memory with ( design system circuit) same attribute	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 18:27
S11 9	39	generat\$3 with logical adj2 (representation description information data) and memory with ( design system circuit) same attribute and specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/20 18:29
S12 3	7254	memory adj system same implement\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:37
S12 4	29290	memory with (system architecture) same programmable	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:38
S12 5	247568	(interconnect\$3 net network) same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:39



## EAST Search History

S12 6	35964	(ASIC programmable adj device FPGA PLD ) same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:41
S12 8	100	(physical layout)adj description with generat\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:42
S13 1	0	S129 and S124	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:43
S13 0	0	S129 and S123	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:43
S12 9	1	S127 and S128	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:43
S13 2	1	S129 and S125	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:44
S13 4	0	S129 and S126 and specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:45
S13 3	1	S129 and S126	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:45

## EAST Search History

S12 7	61	logical adj description with generat\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:52
S13 7	26	logical adj description with generat\$3 and memory with system and specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:56
S13 8	7	logical adj description with generat\$3 and memory with system and specification and attribute	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:57
S13 9	8	logical adj description with generat\$3 and memory and specification and attribute	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:58
S14 0	8	logical adj description with generat\$3 and memory and specification and attribute and (interconnect\$3 connect\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 09:59
S14 7	30	memory with system and generat\$3 with logical adj description	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:28
S14 9	7	memory with system and generat\$3 with logical adj description and attribute and specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:29
S14 8	8	memory with system and generat\$3 with logical adj description and attribute	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:29

## EAST Search History

S15 1	7	memory with system and generat\$3 with logical adj description and attribute and specification and (interconnect\$3 connect\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:30
S15 5	16	message adj processing and programmable adj device and interconnect\$3 and specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:53
S15 4	27	message adj processing and programmable adj device and interconnect\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:53
S55	77469	specification with (reciev\$3 obtain\$3 input provid\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:25
S16 1	1485	S159 and S160	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:30
S16 0	25264	attribute same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:30
S15 9	89907	(receiv\$3 obtain\$3 get\$4 input\$4 ) with specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:30
S16 3	1	S161 and S162	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:32

## EAST Search History

S16 4	2062	(programmable adj device FPGA PLD ) same interconnect\$4 same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:33
S16 6	0	S161 and S164 and S162	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:35
S16 5	19	S161 and S164	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:35
S16 2	180	generat\$3 with logical adj (representation description)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:35
S17 0	4	generat\$3 with logical adj (representation description) and memory and attribute and specification and interconnect\$3 and topology	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:36
S16 8	45	generat\$3 with logical adj (representation description) and memory and attribute and specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:36
S16 9	16	generat\$3 with logical adj (representation description) and memory and attribute and specification and interconnect\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:37
S17 1	86377	(FPGA PLD PLA CPLD programmable adj device) same ( \$5connect\$3 connect\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 17:57

## EAST Search History

S17 2	3159	(API application adj programming adj interface) and S171	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 17:58
S17 6	139	(HDL VHDL verilog hardware adj description adj language) and S172 and memory and (layout physical) and specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 18:01
S17 7	84	(HDL VHDL verilog hardware adj description adj language) and S172 and memory and (layout physical) and specification and attribute	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 18:11
S17 8	116	(HDL VHDL verilog hardware adj description adj language) and S172 and memory and (layout physical) and specification and architecture	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 18:12
S17 9	45307	(specification and attribute and memory)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:22
S18 1	202085	(pla pld cpld fpga programmable adj device)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:23
S18 6	434	S179 and S181 and S182	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:29
S18 5	3123	S179 and S181	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:29

## EAST Search History

S188	50	S179 and S181 and S182 and S183 and S184	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:30
S187	325	S179 and S181 and S182 and S183	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:30
S190	29	S188 and S189	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:31
S192	32	S188 and S191	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:33
S189	139175	interfac\$3 with program\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:33
S194	35	S188 and S193	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:39
S193	454965	interfac\$3 and program\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:39
S191	220635	interfac\$3 same program\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:39

## EAST Search History

S18 4	26367	memory same component same interconnect\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:40
S19 5	144242	memory and component and interconnect\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:41
S19 7	202	S179 and S181 and S182 and S183 and S195 and S193	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:42
S19 6	223	S179 and S181 and S182 and S183 and S195	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:42
S18 2	43850	(generat\$3 obtain\$3 acquir\$3 out\$3 input\$4 receiv\$3 ) with (logical rtl HDL hardware adj description ) with ( data representation description information)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:51
S18 3	68659	(generat\$3 obtain\$3 acquir\$3 out\$3 input\$4 receiv\$3 ) with (physical layout rtl HDL hardware adj description netlist) with ( data representation description information)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:52
S19 8	176	S179 and S181 and S182 and S183 and S195 and S191	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 12:58
S20 0	142	S179 and S181 and S182 and S183 and S195 and S191 and @ad<"20040101"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:01

## EAST Search History

S20 1	120	S179 and S181 and S182 and S183 and S195 and S191 and configurat\$5 and @ad<"20040101"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:13
S20 3	101	S179 and S181 and S182 and S183 and S195 and S191 and configurat\$5 and (primitive basic adj (cell element component block)) and @ad<"20040101"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:18
S20 4	113	S179 and S181 and S182 and S183 and S195 and S191 and configur\$7 and (primitive basic adj (cell element component block)) and @ad<"20040101"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:19
S20 5	50	S179 and S181 and S182 and S183 and S195 and S191 and configur\$7 and (primitive basic adj (cell element component block)) and (process\$3 stor\$3)with (message packet)and @ad<"20040101"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:34
S20 6	56	S179 and S181 and S182 and S183 and S195 and S191 and configur\$7 and (primitive basic adj (cell element component block)) and configur\$7 same (process\$3 stor\$3)same (message packet frame block adj information cell data adj unit)and @ad<"20040101"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:39
S20 8	5520	S207 and S181	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:41
S21 1	102	S207 and S181 and S179 and S182 and S183	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:42
S21 0	152	S207 and S181 and S179 and S182	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:42



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S20 9	642	S207 and S181 and S179	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:42
S21 3	63	S207 and S181 and S179 and S182 and S183 and S191 and S195	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:43
S21 2	74	S207 and S181 and S179 and S182 and S183 and S191	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:43
S20 7	87871	configur\$7 same (process\$3 stor\$3)same (message packet frame block adj information cell data adj unit)and @ad<"20040101"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:45
S21 7	115	S214 and S179 and S181 and S182 and S182	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:47
S21 6	433	S214 and S179 and S181	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:47
S21 5	3959	S214 and S179	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:47
S21 8	20	S214 and S179 and S181 and S182 and S182 and S184	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:50

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S21 9	20	S214 and S179 and S181 and S182 and S182 and S184 and network	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:54
S22 0	20	S214 and S179 and S181 and S182 and S182 and S184 and (computer same ( communication network ))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:56
S21 4	58340	configur\$7 same (process\$3 stor\$3)with (message packet frame block adj information cell data adj unit)and @ad<"20040101"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:57
S22 3	192	S222 and S179 and S180	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:59
S22 2	13604	configur\$7 same (process\$3 stor\$3)with (message packet frame block adj information cell data adj unit)and communication with computer and @ad<"20040101"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:59
S22 4	4	S222 and S179 and S180 and S182 and S183 and S184	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 14:02
S23 1	104	(fpga ASIC PLD programmable adj device) same (stor\$3 receiv\$3 process\$3) with (message frame packet ) same memory with configur\$7 and component and interconnect\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 14:08
S23 4	7	configur\$5 and (fpga pld programmable adj device) and model and header and xml and "716"/\$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 21:24

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S23 5	428	configur\$5 same ( programmable adj device fpga pld pla) same memory and model same memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 10:19
S23 7	126	S235 and S236	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 10:23
S23 6	114660	(requirement specification) and attribute and (receiv\$3 acquir\$3 get\$4 input\$4 obtain\$3 output\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 10:23
S24 0	29	S237 and S238 and generat\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 10:25
S23 9	29	S237 and S238	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 10:25
S23 8	12260	xml and model and memory and system	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 10:25
S24 1	29	S237 and S238 and generat\$3 and implement\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 10:26
S24 2	29	S237 and S238 and generat\$3 and (implement\$3 map\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 10:39

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S24 7	46	memory and system and programming with interfac\$3 and (fpga pla pld programmable adj device) and (hdl rtl netlist logical adj description) same generat\$3 same ( configuration physical)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 17:09
S24 8	15	memory and system and programming with interfac\$3 and (fpga pla pld programmable adj device) and (hdl rtl netlist logical adj description) same generat\$3 same ( configuration physical) and (packet frame)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 17:27
S24 9	11	memory same system and programming with interfac\$3 and (fpga pla pld programmable adj device) and (hdl rtl netlist logical adj description) same generat\$3 same ( configuration physical) and (packet frame) and interconnect\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 17:28
S25 1	11	memory same system and programming with interfac\$3 and (fpga pla pld programmable adj device) and (hdl rtl netlist logical adj description) same generat\$3 same ( configuration physical) and (packet frame) and specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 17:31
S25 0	9	memory same system and programming with interfac\$3 and (fpga pla pld programmable adj device) and (hdl rtl netlist logical adj description) same generat\$3 same ( configuration physical) and (packet frame) and interconnect\$3 and specification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 17:31
S25 2	3944	709/217.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 20:01
S25 3	50012	memory and system and interconnect\$3 and ( data code description) and (logical rtl HDL gate adj2 level) and (physical map\$4 configur\$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 20:21

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S25 4	423	S252 and S253	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 20:22
S25 5	374	S252 and S253 and component	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/28 20:23
S25 7	36	memory adj architecture same component same interconnect	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 23:26
S26 1	31	memory adj architecture same component same interconnect and interface and processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 23:29
S26 0	31	memory adj architecture same component same interconnect and interface	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 23:29
L7	28	message with stor\$3 same memory and (message network) adj2 processor and (plurality multiple) and message with stor\$3 with (plurality multiple) adj2 memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:32
L10	20	memory adj system same (message ) adj2 (processor system) and interface and interconnect\$3 and architecture	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:35
L11	14	memory adj system same (message ) adj2 (processor system) and interface and interconnect\$3 and architecture and configur\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:37

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L13	15	memory adj system and (message ) adj2 (processor system) and interface and interconnect\$3 and memory adj2 architecture and configur\$5 same memory and (programmable adj device pld fpga )	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:39
L14	15	memory adj system and message adj2 (processor system) and interface and interconnect\$3 and memory adj2 architecture and configur\$5 same memory and (programmable adj device pld fpga )	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:41
L16	38	memory and message adj (processor system) and interface and interconnect\$3 and memory adj2 architecture and configur\$5 same memory and (programmable adj device pld fpga )	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:42
S26 3	11	memory adj architecture same memory adj component and interconnect and interface and processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:46
L18	40	memory adj architecture and memory adj component and interconnect and memory adj2 interface and processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:47
L19	35	memory adj architecture and memory adj component and interconnect and memory adj2 interface and processor and (configur\$5 programmable)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:48
L21	34	memory adj architecture and memory adj component and interconnect and memory adj2 interface and processor and (configur\$5 programmable) near5 memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:49
L20	34	memory adj architecture and memory adj component and interconnect and memory adj2 interface and processor and (configur\$5 programmable) with memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:49

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L23	11	memory adj architecture and memory adj component and interconnect and memory adj interface and processor and (configur\$5 programmable) near5 memory and (fpga pld)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:56
L22	12	memory adj architecture and memory adj component and interconnect and memory adj2 interface and processor and (configur\$5 programmable) near5 memory and (fpga pld)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:56
L27	20	memory adj architecture and interconnect and memory adj interface and (configur\$5 programmable) same memory and (fpga pld) and message with processing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/30 16:59